DPC SOUND CHIP. DPC/DAVE/1 ISSUE 5

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The DPC Sound Chip performs the following functions:-

1. Multi-function "3 tones + noise" stereo sound generator.
2. Memory paging.
3. Address decoding for on-board ram,rom and cartridge.
4. Interrupt system including 1Hz and programmable frequency timer interrupts and two external inputs.
5. Reset circuit compatible with Z80 and dynamic ram.
6. I/O strobe signals for use with external octal latches and tri-state buffers.
7. 1MHz system clock.
8. Z80 wait state generator.

DPC sound chip has 22 internal registers, 17 of which are write-only. 16 of these registers are associated with the sound generation, four R/W registers are for memory management, and one R/W register is used for interrupt control. The last write-only register is used for setting the overall system configuration. Internal decoding is provided for a further 3 I/O registers, read and write strobes being brought out for use with external latches and tri-state buffers on the data bus. Reset clears all 22 internal registers.

The 3 tone generators produce square waves with frequency programable from 30Hz to 125KHz which can be modified in various ways:-

a. Distortion can be introduced by using the output frequency to sample H.F. clocked polynomial counters. PN counters which can be selected are 4,5 or 7 bit. The 7 bit PN can also be exchanged for a variable length 17/15/11/9 bit PN counter.
b. A simple high pass filter is provided on each channel, clocked by the output of a different channel.
c. A ring modulator effect is provided on each channel, with the output of a different channel for it's other input.

The noise channel is normally a 17 bit PN counter clocked from 31KHz, generating a pseudo white noise. The input to this counter can be changed to clock off any of the 3 tone channels, and the PN counter can be reduced in length to 15,11 or 9 bits. This counter can also be exchanged for the 7 bit PN counter. The resulting noise is then passed through high pass and low pass filters and a ring modulator, each controlled by the output of a different tone channel.

The 3 tone generator outputs and the noise generator output are routed to 2 amplitude control circuits (left and right). Each amplitude control consists of four 6 bit write-only registers (one for each sound) which are multiplexed onto an external 6 bit D/A resistor network. In it's own time slot each channel outputs the value in it's amplitude register if tone is high, else zero.

Either or both of the sound output channels may be turned into 6 bit D/A outputs, when they will constantly output the values in tone channel 0 amplitude registers. This is controlled by 2 bits in the write-only sound configuration register. Three further bits may be used to synchronise the tone generators by holding them at a preset count until sync bit goes low.

Memory management consists of four read/write registers which may be output onto A14-A21 pins by selecting the required register with A14',A15'. This provides 256 * 16K pages. These outputs may be tri-stated with BREQ.

Four latched interrupts are provided, a 1Hz interrupt for time clock applications, an interrupt switchable between 50Hz, 1KHz, or the outputs of tone generators 0 or 1, and two external negative edge triggered interrupts. Each interrupt latch has it's own enable and reset controlled by an 8 bit write-only register. An attempt to read this register will return the state of the four interrupt latches and two interrupt input pins, and also two flip-flops toggling off the timer interrupts. The setting of any interrupt latch will bring IRQ low (open drain). 50Hz/1KHz/tone generator interrupt selection is made by 2 bits in the sound configuration register.

Select signals are generated for rom, cartridge, video ram and video I/O. A 1MHz clock output is also provided.

A Z80 reset is provided on RSTO, either on switch on by an external RC network on CAP, or a low going signal on RSTI. The latter generates a 1mS reset pulse synchronised to the falling edge of M1 to prevent loss of data stored in dynamic ram. The RSTO output requires an external 74ALS04 inverter to drive the system reset line at the correct speed and inversion.

A write-only system configuration register is used to set the system for 16/64K on board ram, 8/12MHz input clock, and wait states. The wait state generator can be programmed to give no wait states, waits on opcode fetch only, or waits on all memory accesses. Note that no wait is ever generated for access to video ram, as this would conflict with Z80 clock stretch.

REGISTER DESCRIPTIONS

R0 W EA0

b7-b0 Low byte of numoer to be loaded into 12 bit down counter to set period of tone channel 0.

R1 W EA1

b3-b0 High nybble of above. f out = 125,000/(n+1) Hz.

b5,b4
00 = Pure tone.
01 = Enable 4 bit polynomial counter distortion.
10 = " 5 bit " " "
11 = " 7 bit " " "

b6 1 = Enable high pass filter using tone channel 1 as clock.

b7 1 = Enable ring modulator with tone channel 2.

R2 W EA2

As R0 but for tone channel 1.

R3 W EA3

As R1 but for tone channel 1 except:-

H.P.F. uses tone channel 2.
R.M. uses noise channel.

R4 W EA4

As R0 but for tone channel 2.

R5 W EA5

As R1 but for tone channel 2 except:-

H.P.F. uses noise channel.
R.M. uses tone channel 0.

R6 W EA6

b1,b0 Select noise clock frequency:-

00 = 31.25KHz.
01 = tone channel 0.
10 = tone channel 1.
11 = tone channel 2.

b3,b2 Select polynomial counter length:-

00 = 17 bit.
01 = 15 bit.
10 = 11 bit.
11 = 9 bit.

b4 1 = Swop 17 bit and 7 bit polynomial counters.

b5 1 = Enable low pass filter on noise using tone channel 2 as clock.

b6 1 = Enable high pass filter on noise using tone channel 0 as clock.

b7 1 = Enable ring modulator with tone channel 1.

R7 W EA7

b0 Sync for tone channel 0.
(1 = hold at preset, 0 = run).

b1 Sync for tone channel 1.

b2 Sync for tone channel 2.

b3 1 = Turn L.H. audio output into D/A, outputing value in R8.

b4 1 = Turn R.H. audio output into D/A, outputing value in R12.

b6,b5 Select interrupt rate:-

00 = 1KHz.
01 = 50Hz.
10 = Tone generator 0. f = 250,000/(n+1)
11 = Tone generator 1.

b7 Undefined.

R8 W EA8

b5-b0 Tone channel 0 L.H. amplitude.
Also value output to L.H. D/A if R7 b3 = 1.

b7,b6 Undefined.

R9 W EA9

b5-b0 Tone channel 1 L.H. amplitude.

b7,b6 Undefined.

R10 W EAA

b5-b0 Tone channel 2 L.H. amplitude.

b7,b6 Undefined.

R11 W EAB

b5-b0 Noise channel L.H. amplitude.

b7,b6 Undefined.

R12 W EAC

b5-b0 Tone channel 0 R.H. amplitude.
Also value output to R.H. D/A if R7 b4 = 1.

b7,b6 Undefined.

R13 W EAD

b5-b0 Tone channel 1 R.H. amplitude.

b7,b6 Undefined.

R14 W EAE

b5-b0 Tone channel 2 R.H. amplitude.

b7,b6 Undefined.

R15 W EAF

b5-b0 Noise channel R.H. amplitude.

b7,b6 Undefined.

R16 R/W £B0

b7-b0 Page register output to A21-A14 if A15',A14' = 00

R17 R/W £B1

b7-b0 Page register output to A21-A14 if A15',A14' = 01

R18 R/W £B2

b7-b0 Page register output to A21-A14 if A15',A14' = 10

R19 R/W £B3

b7-b0 Page register output to A21-A14 if A15',A14' = 11

R20 W £B4

b0 1 = Enable 1KHz/50Hz/TG interrupt.

b1 1 = Reset 1KHz/50Hz/TG interrupt latch.

b2 1 = Enable 1Hz interrupt.

b3 1 = Reset 1Hz interrupt latch.

b4 1 = Enable INT1.

b5 1 = Reset INT1 latch.

b6 1 = Enable INT2.

b7 1 = Reset INT2 latch.

R20 R £B4

b0 1KHz/50Hz/TG divider. (f int/2 square wave).

b1 1 = 1KHz/50HZ/TG latch set.

b2 1 Hz divider. (0.5 Hz square wave).

b3 1 = 1Hz latch set.

b4 INT1 input pin.

b5 1 = INT1 latch set.

b6 INT2 input pin.

b7 1 = INT2 latch set.

R21 W £35

Active low strobe on WR0.

R21 R £35

Active low strobe on RD0.

R22 W £36

Active low strobe on WR1.

R22 R £36

Active low strobe on RD1.

R23 W £37

Active low strobe on WR2.

R23 R £37

Active low strobe on RD2.

R31 W £3F

b0	On board ram. 0 = 64k, 1 = 16k.
b1	Input clock frequency. 0 = 8MHz, 1 = 12MHz.
b3,b2	00 = Wait on all memory access except video ram. 01 = Wait on M1 only, except video ram. 10 = No waits. 11 = No waits.

SELECT OUTPUTS

VIO	Low for I/O access £80 to £8F. Gated with IORQ,RD,WR in video chip.
ROM	Low for memory access on pages 0-3.(0-£FFFF) Gated externally with RD.
CART	Low for memory access on pages 4-7.(£10000-£1FFFF) Gated externally with RD,WR
VRAM	Low for any memory access on pages £FC-£FF (£3F0000-£3FFFFF) IF R31 b0 = 0.
-	Low for any memory access other than rom or cartridge (£20000-£3FFFFF) IF R31 b0 = 1.
	Gated with MREQ,RD,WR in video chip.